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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,271	01/25/2001	Tsukasa Yajima	PNET.009D	3802

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,271	YAJIMA, TSUKASA	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-9,11-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-9,11-13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/25/2001
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 09, 2005 has been entered.

Status of the Claims

2. Amendment filed November 09, 2005 has been entered. Claim 14 has been cancelled. Claims 6, 11 and 16 have been amended. Claims 6-9, 11-13 and 15-19 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 6-9 and 11-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "sidewall spacers of silicon oxide film formed on the side surfaces of said first and second gates, and **not on the**

side surfaces of said protective layer" (as recited in amended claims 1, 11 and 16) in the application as filed.

Since the drawing is only an illustration of the invention, a limitation of the claim must have support in the original specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6-9 and 11-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "sidewall spacers of silicon oxide film formed on the side surfaces of said first and second gates, and **not on the side surfaces of said protective layer**" (as recited in amended claims 1, 11 and 16) is a *negative limitation* that renders the claims indefinite because it was an attempt to claim the invention by excluding what the inventor *did not invent* rather than distinctly and particularly pointing out what they did invent. See *In re Schechter*, 205 F.2d 185, 98 USPQ 144 (CCPA 1953). (See MPEP 2173.05(i)). Any negative limitation or exclusionary proviso *must have* basis in the original disclosure. See *In re Johnson*, 558 F.2d 1008, 1019, 194 USPQ 187, 196 (CCPA 1977).

5. Claims 16-19 are further rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites: sidewall spacers of silicon oxide film formed on the side surfaces of said protective layer; and not on the side surface of said protective layer.

As best understood by the examiner, the sidewall spacers are not formed on the side surfaces of the field oxide.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoo et al. (U.S. Patent No. 5,605,853) of record.

With respect to claim 16, as best understood by the examiner, Yoo teaches a semiconductor device as claimed including:

a gate (16) formed on an active region of a substrate (10), the gate (16) consisting of a refractory metal layer (24) on a polysilicon layer and having side surfaces;

a field oxide (12) formed on the substrate (10) adjacent the active region;

a protective layer (21) formed on the field oxide (12) to prevent overetching of the field oxide, the protective layer (21) being a conductive layer and having side surfaces thereof over the field oxide (12);

sidewall spacers (20) of silicon oxide film formed on the side surfaces of the protective layer; and not on the side surface of the field oxide (12); and

an insulating layer (38), a contact hole, and a connecting wire (40) formed above the surface of the substrate (1),

the protective layer (21) being formed on the field oxide (12) only. (See Fig. 7).

With respect to claim 17, the protective layer (21) of Yoo is a polysilicon layer.

With respect to claim 18, the gate (16) of Yoo is a MOSFET gate.

With respect to claim 19, the semiconductor device of Yoo further comprises an additional gate (16) formed on the substrate (10), the field oxide (12) being formed on the substrate between the gate (16) and the additional gate (16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-9, 11-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watabe (U.S. Patent No. 5,525,530) in view of Amakawa (JP. Patent No. 02-257637) of record.

With respect to claim 6, as best understood by the examiner, Watabe teaches a semiconductor device substantially as claimed including:

first (67) and second (69) gates formed on an active regions of a substrate (1), the first and second gates each consisting of a refractory metal layer (93) on a polysilicon layer (51);

a field oxide (15) formed on the substrate (1) between the first (67) and second gate (69);

sidewall spacers (77) of silicon oxide film (771) formed on the side surfaces of the first (67) and second (69) gates, and not on the surface of the field oxide (15); and

an insulating layer (39), a contact hole, and a connecting wire (40) formed above the surface of the substrate (1). (See Fig. 43).

Thus, Watabe is shown to teach all the features of the claim with the exception of an addition of the a protective layer formed selectively on the field oxide.

However, Amakawa teaches forming an element isolation including a protective layer of polysilicon (hence conductive) film (7) being formed selectively on and having side surfaces over the field oxide (6) to prevent a reduction in thickness of the field oxide (6) for element isolation use in the subsequence process. (See Fig. 1e and Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a protective layer on the field oxide of Watabe as taught by Amakawa to prevent thinning of the field oxide thus maintaining a desired isolation withstand voltage.

Product by process limitation:

The expression "to prevent overetching of said field oxide" (claims 6, 11 and 16) is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at

17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With respect to claim 11, as best understood by the examiner, Watabe teaches a semiconductor device as claimed including:

a gate (67) formed on an active region of a substrate (1), gate (67) having side surfaces;

a field oxide (15) formed on the substrate (1) adjacent the active region;

sidewall spacers (77) formed on the side surfaces of gate (67), and not on the surface of the field oxide (15); and

an insulating layer (39), a contact hole, and a connecting wire (40) formed above the surface of the substrate (1). (See Fig. 43).

Thus, Watabe is shown to teach all the features of the claim with the exception of an addition of the a protective layer formed on the field oxide only.

However, Amakawa teaches forming an element isolation including a protective layer of polysilicon (hence conductive) film (7) being formed only on and having side surfaces over the

field oxide (6) to prevent a reduction in thickness of the field oxide (6) for element isolation use in the subsequence process. (See Fig. 1e and Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a protective layer on the field oxide of Watabe as taught by Amakawa to prevent thinning of the field oxide thus maintaining a desired isolation withstand voltage.

With respect to claims 7 and 12 the protective layer (7) of Amakawa is a polysilicon layer.

With respect to claim 8, the protective layer (7) of Amakawa is formed on the field oxide (6) only.

With respect to claims 9 and 13, the gates (67,69) of Watabe are a MOSFET gate.

With respect to claim 15, the semiconductor device of Watabe further comprising an additional gate (69) formed on the substrate (1), the field oxide (15) being formed on the substrate (1) between the gate (67) and the additional gate (69).

Response to Arguments

8. Applicant's arguments filed November 09, 2005 have been fully considered but they are not persuasive.

Rejection under 35 U.S.C. 112, first paragraph:

Arguing the present of the sidewall spacers, Applicant asserts: "That is, the application reasonably conveys a structure including sidewalls on side surfaces of a gate, and not on side surfaces of a protective layer formed on a field oxide layer".

This is purely a conclusion that disregards the fundamental of scientific foundation.

The specification is completely silence regarding the present of the sidewall spacers on the protective layer.

Yoo '853, as shown in Fig. 2, col. 4, lines 9-14, clearly states: sidewall spacers 20 and 20' are now formed adjacent to the polysilicon structures, by depositing an insulating material such as SiO_2 (silicon oxide) and performing an *anisotropic etch* to remove the oxide in all but the sidewall regions, **as is known in the art**.

The instant specification describes an exact same process. However, the amended claims 6, 11 and 16 attempted to exclude the present of the sidewall spacers on the side surface of the protective layer, e.g. not on the side surfaces of said protective layer, which the specification fails to indicate. (Page 13, line 18 to page 14, line 12). The focus of the instant invention is to protect the field oxide utilizing the protective layer, not the present or absent of the sidewall spacers on the side surfaces of the protective layer. Given the amount of information, one having ordinary skill in the art should have concluded that sidewall spacers should exist on the side surfaces of the protective layer as well as the gate electrodes.

Applicant also requests this Examiner to provide case law in support for maintaining the non-compliance rejection.

MPEP 2163 clearly states: "the analysis of whether the specification complies with the written description requirement calls for the examiner to compare the scope of the claim with the scope of the description to determine whether the applicant has demonstrated possession of the claimed invention. Such a review is conducted from the standpoint of one of skill in the art at the

time of the applicant was filed (see, e.g., *Wang Labs. v. Toshiba Corp.*, 993 F.2d 858, 865, 26 USPQ2d 1767, 1774 (Fed. Cir. 1993)) and should include a determination of the field of the invention and the level of skill and knowledge in the art".

Comparing the scope of the claim and the scope of the description, it is clear that applicant does not demonstrated possession of the claimed invention, e.g., spacers are formed on the side surfaces of the gate but not on that of the protective layer.

From the standpoint of one of skill in the art at the time of the applicant was filed, it is fair to conclude that an anisotropic etch, including overetch, that forms sidewall spacers on the side surfaces of the gate electrode also forms sidewall spacers on the side surfaces of the protective layer.

Furthermore, applicant has put on record that sidewall spacers does exist on the side surfaces of the protective layer. (See claim 16).

Rejection under 35 U.S.C. 112, second paragraph:

MPEP 2173.05(i) clearly indicates: "any negative limitation or exclusionary proviso must have basis in the original disclosure. If alternative elements are positively recited in the specification, they may be explicitly excluded in the claims. See *In re Johnson*, 558 F2.d 1008, 1019, 194 USPQ 187, 196 (CCPA 1997)".

A complete silence on the sidewall spacers of the protective layer in the specification is not deem as a positive recitation.

9. Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER